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A clock regeneration circuit for regenerating a clock signal for demodulating data from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of an amplitude-modulated signal at the same time. The carrier for an amplitude-modulated signal is extracted from an AM data multiplex modulated signal where digitally modulated signals are multiplexed in the same frequency band as those of the amplitude-modulated signal at the same time through a band-pass filter (1), and the oscillation frequency of a voltage-controlled oscillator (5) is controlled by the output of a phase comparator (3) through a loop filter (4). The oscillation output of the voltage-controlled oscillator (5) is supplied to a direct digital synthesizer (6) and the phase of the carrier extracted through the band-pass filter (1) is compared with the phase of the output of the direct digital synthesizer (6) by means of the phase comparator (3). The oscillation output of the voltage-controlled oscillator (5) is then synchronized with the carrier for the amplitude-modulated signal to produce a clock signal for demodulating data.

